

## CLAIMS

*What is claimed is:*

1. A conductive memory device comprising:

a conductive bottom electrode;

a multi-resistive state element arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes; and

wherein at least one of the conductive electrodes functions as a barrier layer.

2. The conductive memory device of claim 1, wherein:

the multi-resistive state element is fabricated with high temperature processes.

3. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer includes either titanium or titanium nitride.

4. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer additionally functions as an adhesion layer.

5. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer includes a binary nitride.

6. The conductive memory device of claim 5, wherein:

the binary nitride is either titanium nitride, tantalum nitride or tungsten nitride.

7. The conductive memory device of claim 5, wherein:

the binary nitride reduces either metal diffusion, oxygen diffusion, hydrogen diffusion, or some combination thereof.

8. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer includes a ternary nitride.

9. The conductive memory device of claim 8, wherein:

the ternary nitride is either titanium silicon nitride, tantalum aluminum nitride, titanium aluminum nitride, or tantalum silicon nitride.

10. The conductive memory device of claim 9, wherein:

the ternary nitride reduces either metal diffusion, oxygen diffusion, hydrogen diffusion, or some combination thereof.

11. The conductive memory device of claim 8, wherein:

the ternary nitride has one component that is either ruthenium or iridium and another component that is either tantalum or titanium.

12. The conductive memory device of claim 11, wherein:

the ternary nitride is ruthenium titanium nitride.

13. The conductive memory device of claim 11, wherein:

the ternary nitride functions as a sacrificial high-temperature oxygen barrier.

14. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer includes a ternary oxide.

15. The conductive memory device of claim 14, wherein:

the ternary oxide has one component that is either ruthenium or iridium and another component that is either tantalum or titanium.

16. The conductive memory device of claim 15, wherein:

the ternary oxide is ruthenium tantalum oxide.

17. The conductive memory device of claim 14, wherein:

the ternary oxide acts as a sacrificial high-temperature oxygen barrier, whereby the at least one of the conductive electrodes remains conductive after the ternary oxide reacts with oxygen.

18. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer includes a conductive oxide.

19. The conductive memory device of claim 18, wherein:

the conductive oxide is  $\text{LaSrCoO}_3$ ,  $\text{RuO}_2$ ,  $\text{IrO}_2$ ,  $\text{SrRuO}_3$ ,  $\text{LaNiO}_3$  or a doped STO.

20. The conductive memory device of claim 18, wherein:

a portion of the at least one of the conductive electrodes that functions as a barrier layer includes a conductive oxide and another portion of the at least one of the conductive electrodes that functions as a barrier layer includes a non-oxidized conductor such that the conductive oxide is an oxidized form of the non-oxidized conductor.

21. The conductive memory device of claim 18, wherein:

the conductive oxide is a conductive metal that is oxidized during fabrication and remains conductive after oxidation.

22. The conductive memory device of claim 21, wherein:

the metal is Ir or Ru.

23. The conductive memory device of claim 18, wherein:

the conductive oxide modifies the formation of oxygen vacancies in the multi-resistive state element.

24. The conductive memory device of claim 18, wherein:

the conductive oxide modifies the migration of oxygen vacancies in the multi-resistive state element.

25. The conductive memory device of claim 18, wherein:

the multi-resistive state element is fabricated with high temperature processes.

26. The conductive memory device of claim 18, wherein:

the conductive oxide does not degrade due to oxidation.

27. The conductive memory device of claim 18, wherein:

the bottom electrode is fabricated prior to the multi-resistive state material;

the at least one of the conductive electrodes that functions as a barrier layer is the bottom electrode; and

the bottom electrode functions as a seed layer to the multi-resistive state material.

28. The conductive memory device of claim 27, wherein:

the bottom electrode causes the multi-resistive state material to have a lowered crystallization temperature.

29. The conductive memory device of claim 18, wherein:

the at least one of the conductive electrodes that functions as a barrier layer includes a layer of metal in between the conductive oxide and the multi-resistive state element.

30. The conductive memory device of claim 29, wherein the metal is platinum.

31. The conductive memory device of claim 29, wherein the layer of metal introduces a non-linearity in the IV characteristics of the conductive memory device.

32. The conductive memory device of claim 1, wherein:

the top electrode, the multi-resistive state element, and the bottom electrode each have similar coefficients of thermal expansion, whereby the conductive memory element does not experience significant stress from dissimilar coefficients of thermal expansions during normal operation.

33. The conductive memory device of claim 1, wherein:

at least one of the bottom electrode, the multi-resistive state element, or the top electrode is protected by an insulating barrier.

34. The conductive memory device of claim 33, wherein:

the insulating barrier includes silicon nitride.

35. The conductive memory device of claim 33, wherein:

the insulating barrier includes aluminum oxide.

36. The conductive memory device of claim 33, wherein:

the insulating barrier includes titanium oxide.

37. The conductive memory device of claim 1, wherein:

the at least one of the conductive electrodes that functions as a barrier layer is the bottom electrode; and

the top electrode is a non-oxidized metal.

38. A conductive memory device, comprising:

a memory element that stores an adjustable resistive value;

two electrodes that deliver current to the memory element;

wherein at least one electrode includes a terminal layer that is suitable for connecting the electrode to either a conductive line or a transistor terminal;

wherein the at least one electrode has an outside face that is defined by the terminal layer and an inside face opposite the outside face; and

wherein the at least one electrode acts as a barrier layer.

39. The conductive memory device of claim 38, wherein:

only a portion of the at least one electrode acts as barrier layer, the portion being located away from the outside face.

40. The conductive memory device of claim 38, wherein:

only a portion of the at least one electrode acts as barrier layer, the portion being located away from the inside face.

41. A re-writable memory comprising:

a substrate;

a plurality of circuits on the substrate;

a plurality of x-direction conductive lines in oriented in one direction;

a plurality of y-direction conductive lines in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines;

at least one memory array formed by memory cells placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines;

wherein each memory cells in the memory array includes at least one electrode that acts as a barrier layer.

42. The re-writable memory of claim 41, wherein each memory cell includes a memory element that stores an adjustable resistive value.

43. The re-writable memory of claim 42, wherein each memory cell includes a conductive metal oxide memory element that stores an adjustable resistive value.